PRELIMINARY

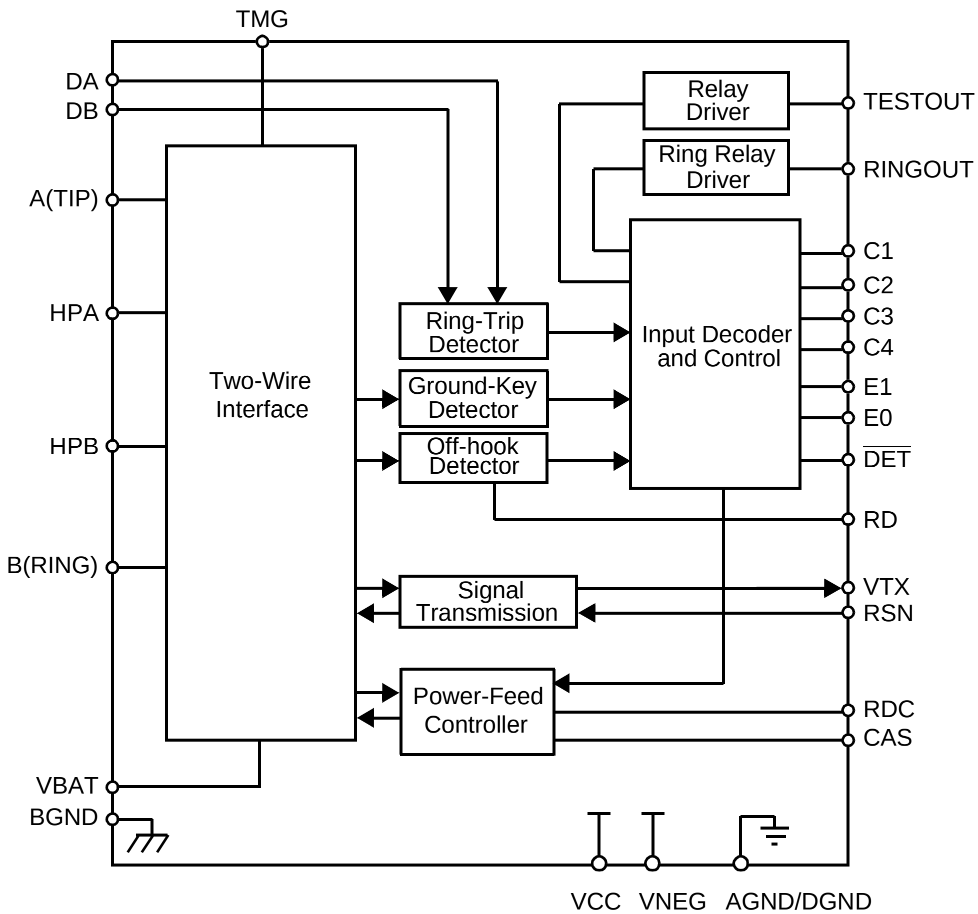
Am79484

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- **Ideal for long-loop applications**
- **Low standby power (45 mW)**
- **–40 V to –58 V battery operation**
- **On-hook transmission**
- **Tip Open state for ground-start lines**
- **Two-wire impedance set by single external impedance**
- **Programmable constant-current feed**
- **Programmable loop-detect threshold**
- **Current gain = 200**
- **Polarity reversal option available**
- **On-chip Thermal Management (TMG) feature**
- **On-chip ring and test relay driver and relay snubber circuits**

BLOCK DIAGRAM



Publication# **20755** Rev: **B** Amendment: **/0**
Issue Date: **July 1998**

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am79484 –1 J C

TEMPERATURE RANGE
C = Commercial (0°C to 70°C)*

PACKAGE TYPE
J = 32-pin Plastic Leaded Chip Carrier (PL 032)

PERFORMANCE GRADE OPTION
–1 = 52 dB Longitudinal Balance, Polarity Reversal
–2 = 63 dB Longitudinal Balance, Polarity Reversal
–3 = 52 dB Longitudinal Balance, No Polarity Reversal
–4 = 63 dB Longitudinal Balance, No Polarity Reversal

DEVICE NUMBER/DESCRIPTION
Am79484
Subscriber Line Interface Circuit

Valid Combinations		
Am79484	–1 –2 –3 –4	JC

Valid Combinations

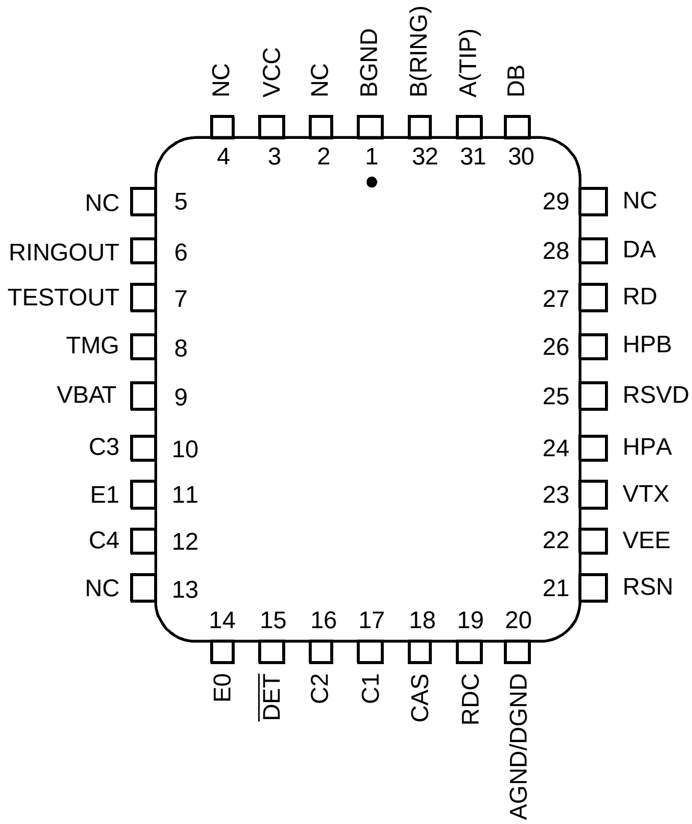
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note:
** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAM

Top View

32-Pin PLCC



Notes:

1. *Pin 1 is marked for orientation.*
2. *NC = No Connect*
3. *RSVD = Reserved. Do not connect to this pin.*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground are connected internally to a single pin.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C4–C1	Inputs	Decoder. TTL compatible. C4 is MSB and C1 is LSB.
CAS	Capacitor	Anti-saturation capacitor. Filters reference voltage when operating in anti-sat region.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{DET}$	Output	Detector. Logic Low indicates that the selected detector is tripped. Logic inputs C3–C1 and E0 select the detector. Open-collector with a built-in 15 kΩ pull-up resistor.
E0	Input	A logic High enables $\overline{DET}$. A logic Low disables $\overline{DET}$.
E1	Input	E1 = High connects the ground-key detector to $\overline{DET}$, and E1 = Low connects the off-hook or ring-trip detector to $\overline{DET}$.
HPA	Capacitor	High-pass filter capacitor; A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor; B(RING) side of high-pass filter capacitor.
NC	—	Pin not internally connected.
RD	Resistor	Detector resistor. Threshold modification/filter point for the off-hook detector.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network, which also connects to the receiver summing node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring relay driver. Open collector Darlington pull down.
RSN	Input	The metallic current (AC and DC) between A(TIP) and B(RING) = 200 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
RSVD	—	This pin is reserved only for test purposes. Leave unconnected.
TESTOUT	Output	Test relay driver. Open collector Darlington pull down.
TMG	—	Thermal management; External resistor connects between this pin and VBAT to off-load power dissipation from SLIC. Functions during Normal Polarity and Reverse Polarity states.
VBAT	Battery	Battery supply. Connected through an external protection diode.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VTX	Output	Transmit Audio; Unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . –55°C to +150°C

V_{CC} with respect to AGND/DGND . . . . –0.4 V to +7 V

V_{EE} with respect to AGND/DGND . . . . +0.4 V to –7 V

V_{BAT} with respect to AGND/DGND:

Continuous . . . . +0.4 V to –70 V
10 ms . . . . +0.4 V to –75 V

BGND with respect to AGND/DGND . . . . +3 V to –3 V

A(TIP) or B(RING) to BGND:

Continuous . . . . –70 V to +1 V
10 ms (f = 0.1 Hz) . . . . –70 V to +5 V
1 µs (f = 0.1 Hz) . . . . –80 V to +8 V
250 ns (f = 0.1 Hz) . . . . –90 V to +12 V

Current from A(TIP) or B(RING). . . . . ±150 mA

RINGOUT/TESTOUT current. . . . . 75 mA

RINGOUT/TESTOUT voltage . . . . BGND to +7 V

RINGOUT/TESTOUT transient . . . . . BGND to +10 V

DA and DB inputs

Voltage on ring-trip inputs . . . . V_{BAT} to 0 V
Current into ring-trip inputs . . . . ±10 mA

C4–C1, E0, E1

Input voltage. . . . . –0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, continuous,

T_A = 70°C, No heat sink (See note):

In 32-pin PLCC package . . . . 1.7 W

Thermal Data: . . . . θ_{JA}

In 32-pin PLCC package . . . . 43°C/W typ

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature, and operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . 0°C to +70°C*

V_{CC} . . . . 4.75 V to 5.25 V

V_{EE} . . . . –4.75 V to –5.25 V

V_{BAT} . . . . –40 V to –58 V

AGND/DGND . . . . 0 V

BGND with respect to
AGND/DGND . . . . –100 mV to +100 mV

Load resistance on VTX to ground . . . . 10 kΩ min

The operating ranges define those limits between which the functionality of the device is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units. Steady state operation at T_A = 70°C is guaranteed by testing at 90°C and guard banding.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz	26			dB	1, 4, 7
Analog output (V_{TX}) impedance			3	20	Ω	4
Analog (V_{TX}) output offset voltage	0°C to +70°C –40°C to +85°C	–40 –50		+40 +50	mV	— 4
Overload level, 2 wire and 4 wire	Active state	2.5			Vpk	2a
Overload level	On hook, R_{LAC} = 900 Ω	1.18			Vrms	2b
THD, Total Harmonic Distortion	0 dBm 0 dBm, R_{LDC} = 2030 Ω, BAT = –42.5 V +7 dBm		–64 –45 –55	–50 –40	dB	5 — 5
THD, on hook	+1 dBm, R_{LAC} = 900 Ω			–36		5
Longitudinal Capability (See Test Circuit C)						
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz –1, –3*	52	70			
	200 Hz to 1 kHz –2, –4* Normal polarity	63				
	200 Hz to 1 kHz –2* Reverse polarity	58				
	200 Hz to 1 kHz –2, –4* –40°C to +85°C	58				4
	1 kHz to 3.4 kHz –1, –3*	52				
	1 kHz to 3.4 kHz –2, –4*	58				
	1 kHz to 3.4 kHz –40°C to +85°C	54				4
Longitudinal signal generation 4-L	200 Hz to 800 Hz Normal polarity	40			dB	
Longitudinal current per pin	Active state Standby state	8.5 8.5	27 27		mArms	
Longitudinal impedance at A or B	0 Hz to 100 Hz		25	35	Ω/pin	
Idle Channel Noise						
C-message weighted noise	+25°C to +85°C –40°C to +25°C		+7	+10 +12	dBrnC	— 4
Psophometric weighted noise	+25°C to +85°C –40°C to +25°C		–83	–80 –78	dBmp	
Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B)						
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C 0 dBm, 1 kHz –40°C to +85°C On hook, OHT state	–0.15 –0.20 –0.35		+0.15 +0.20 +0.35	dB	— 4 4
Gain accuracy over frequency relative to 1 kHz	300 Hz to 3.4 kHz 0°C to +70°C 300 Hz to 3.4 kHz –40°C to +85°C	–0.10 –0.15		+0.10 +0.15		5 4
Gain tracking relative to 0 dBm	+3 dBm to –55 dBm 0°C to +70°C +3 dBm to –55 dBm –40°C to +85°C +3 dBm, BAT = –42.5 V, R_{LDC} = 2030 Ω On hook	–0.10 –0.15 –0.30 –0.35		+0.10 +0.15 +0.30 +0.35		— 4 — —

Note:
** Performance Grade*

ELECTRICAL SPECIFICATIONS (continued)

Description	Test Conditions (See Note 1)		Min	Typ	Max	Unit	Note
Balance Return Signal (4-Wire to 4-Wire)							
Gain accuracy	Ref: 0 dBm, 1 kHz Ref: 0 dBm, 1 kHz	0°C to +70°C –40°C to +85°C	–0.15 –0.20		+0.15 +0.20	dB	3 4
Gain accuracy over frequency	300 Hz to 3400 Hz 300 Hz to 3400 Hz	0°C to +70°C –40°C to +85°C	–0.10 –0.15		+0.10 +0.15	dB	3 4
Gain tracking relative to 0 dBm	+3 dBm to –55 dBm +3 dBm to –55 dBm	0°C to +70°C –40°C to +85°C	–0.10 –0.15		+0.10 +0.15	dB	— 4
Group delay	0 dBm, 1 kHz			4		µs	4, 7
Line Characteristics							
Voltage on TMG pin	Constant-current region			V_{TMG}			8
I_L, short loops, Active or OHT state			20	22	24	mA	
I_L, long loops, Active state	R_{LDC} = 2030 Ω, BAT = –42.5 V, T_A = 25°C		18	18.6		mA	
I_L, accuracy, Standby state	$I_L = \frac{\lvert V_{BAT}\rvert - 3\ V}{R_L + 400}$ Constant-current region	T_A = 25°C	$0.8I_L$ 16	I_L 22	$1.2I_L$ 39	mA	
I_L, loop current, Tip Open state	R_L = 0 Ω, V_A = 0 Ω to V_A = V_{BAT} B to ground V_{BAT} = –56.5 V, R = 2.2 kΩ, B to gnd			0 23 22	100 45 24.5	µA mA mA	
I_L, loop current, Open Circuit state	R_L = 0 Ω				100	µA	
I_LLIM	Active, A and B to gnd			95	120	mA	
V_A, Active, ground-start signaling	A to –48 V = 7 kΩ, B to gnd = 100 Ω		–7.5	–5		V	4
V_{AB}, Open Circuit voltage	BAT = –52 V		–42.75	–45.7		V	
A lead impedance, Tip Open state	V_A = 0 V to V_A = V_{BAT}		150 k	10 M		Ω	4
Power Supply Rejection Ratio (V_{RIPPLE} = 100 mVrms), Active Normal State							
V_{CC}	50 Hz to 3400 Hz 500 Hz to 3000 Hz		30 35	40		dB	5
V_{EE}	50 Hz to 3400 Hz 500 Hz to 3000 Hz		28 30	35		dB	5
V_{BAT}	50 Hz to 3400 Hz 500 Hz to 3000 Hz		28 45	50		dB	5
Effective internal resistance	CAS pin to gnd		85	170	255	kΩ	4
Control lead feed through	50 Hz to 3400 Hz on C1, C2, or C3		35	50		dB	4

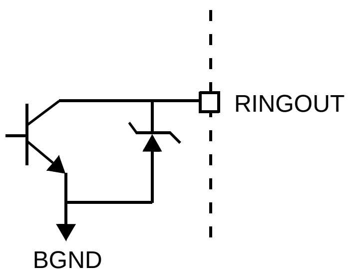
ELECTRICAL SPECIFICATIONS (continued)

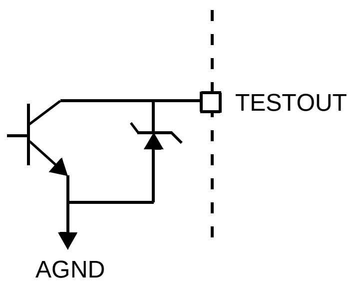
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Power Dissipation						
On hook, Open Circuit state			25	70	mW	
On hook, Standby state			45	85		
On hook, OHT state			180	270		
On hook, Active state	R_{TMG} = open R_{TMG} = 2500 Ω		180 195	270 300		4
Off hook, Standby state			860	1100		
Off hook, OHT state	R_L = 300 Ω, R_{TMG} = open		1000	1300		
Off hook, Active state	R_L = 300 Ω, R_{TMG} = 2500 Ω		450	800		
Supply Currents, Battery = –58 V						
ICC, On-hook V_{CC} supply current	Open Circuit state OHT state Standby state Active state, BAT = –48 V		1.7 7.0 3.0 6.3	2.5 8.5 3.5 8.5	mA	
IEE, On-hook V_{EE} supply current	Open Circuit state OHT state Standby state Active state, BAT = –48 V		0.7 2.0 0.77 2.1	2.0 3.5 2.0 5.0		
IBAT, On-hook V_{BAT} supply current	Open Circuit state OHT state Standby state Active state, BAT = –48 V		0.18 1.9 0.45 4.2	1.0 4.7 1.5 5.7		
RFI Rejection						
RFI rejection	100 kHz to 30 MHz, (See Figure E)			1.0	mVrms	4
Receive Summing Node (RSN)						
RSN DC voltage	I_{RSN} = 0 mA		0		V	4
Logic Inputs (C4–C1, E0, E1)						
V_{IH}, input High voltage		2.0			V	
V_{IL}, input Low voltage				0.8		
I_{IH}, input High current		–75		40	µA	
I_{IL}, input Low current	C4–C1, E0, E1	–400				
Logic Output ($\overline{DET}$)						
V_{OL}, output Low voltage	Iout = 0.3 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, output High voltage	Iout = –0.1 mA, 15 kΩ to V_{CC}	2.4				
Ring-trip Detector Input (DA, DB)						
Bias current		–20	–5		nA	4
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Offset voltage	Source resistance mismatch = 3 MΩ	–50	0	+50		4

ELECTRICAL SPECIFICATIONS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Relay Driver Output (RINGOUT)						
On voltage	I_{OL} = 41 mA		+0.35	+1.00	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.2		V	
Zener ON voltage	I_Z = 30 mA		10			
Test Driver Output (TESTOUT)						
On voltage	I_{OL} = 81.5 mA		+0.8	+1.50	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.2		V	
Zener ON voltage	I_Z = 80 mA		14			
Detector Thresholds						
I_T, loop-detect threshold tolerance	R_D = 35.4 kΩ, Active Standby	$330/R_D$ $330/R_D$	$375/R_D$ $375/R_D$	$420/R_D$ $420/R_D$	A	
I_T, ground-key detect threshold	Tip Open, B lead only, E1 = 0	7.5	10	14	mA	

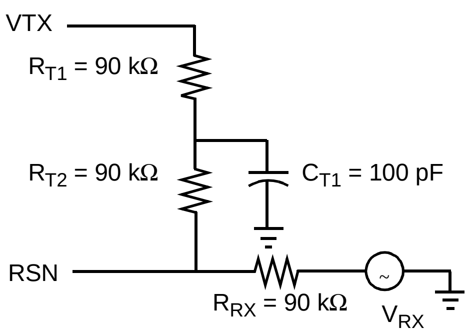
RELAY DRIVER SCHEMATICS





Notes:

1. *Unless otherwise noted, test conditions are BAT = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 11.36 kΩ, R_D = 35.4 kΩ, R_{TMG} = 2.5 kΩ, no fuse resistors, C_{HP} = 0.2 µF, C_{DC} = 0.1 µF, C_{CAS} = 0.1 µF, two-wire AC input impedance is a 900 Ω resistance synthesized by the programming network shown below.*



2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.

3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Group delay can be greatly reduced by using a ZT network such as that shown in Note 1 above. The network reduces the group delay to less than 2 µs and increases 2WRL. The effect of group delay on linecard performance may also be compensated by synthesizing complex impedance with the QSLAC™ or DSLAC™ device.*
8. *The voltage on the TMG pin (V_{TMG}) is related to the voltage across the line (V_{AB}) when the device is in the constant-current region. The relationship between V_{AB} and V_{TMG} voltage is described by the following equation: $V_{TMG} = -0.982|V_{AB}| - 7.85$*

Table 1. SLIC Decoding

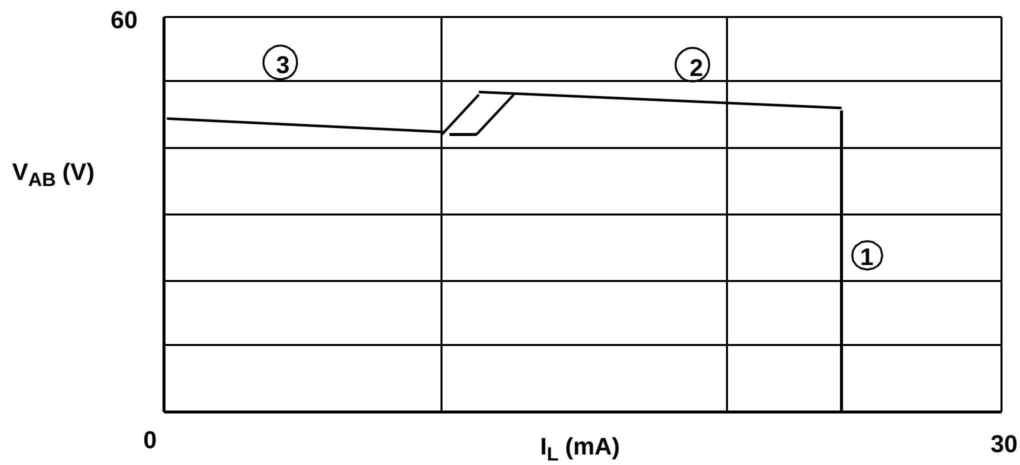
					$\overline{DET}$ Output	
State	**C3**	**C2**	**C1**	**Two-Wire Status**	**E1 = 1**	**E1 = 0**
0	0	0	0	Open Circuit	Ring trip	Ring trip
1	0	0	1	Ringing	Ring trip	Ring trip
2	0	1	0	Active	Loop detector	Ground key
3	0	1	1	On-hook TX (OHT)	Loop detector	Ground key
4	1	0	0	Tip Open	Loop detector	Ground key
5	1	0	1	Standby	Loop detector	Ground key
6	1	1	0	Active Polarity Reversal	Loop detector	Ground key
7	1	1	1	OHT Polarity Reversal	Loop detector	Ground key

Notes:
1. *C4 logic high enables the TESTOUT relay driver.*
2. *E0 logic high enables the $\overline{DET}$ pin.*

Table 2. User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{200 \bullet Z_T}{Z_T + 200(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{500}{I_{LOOP}}$ $C_{DC} = 1.5\text{ ms} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1}R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$R_D = \frac{375}{I_T}, \quad C_D = \frac{0.5\text{ ms}}{R_D}$	R_D and C_D form the network connected from RD to –5 V, and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor, and f_c is the desired filter cut-off frequency.
$I_{OHT} = \frac{500}{R_{DC1} + R_{DC2}}$	OHT loop current (constant-current region).
Thermal Management Equations (Normal Active and Tip Open States)	
$R_{TMG} \geq \frac{\lvert V_{BAT}\rvert - 6\text{ V}}{I_{LOOP}}$	R_{TMG} is connected from T_{MG} to V_{BAT} and is used to limit power dissipation within the SLIC in Active and Tip Open states only.
$P_{RTMG} = \frac{(\lvert V_{BAT}\rvert - 6\text{ V} - (I_L \bullet R_L))^2}{R_{TMG}}$	Power is dissipated in the thermal management resistor, R_{TMG}, during Active and Tip Open states.
$P_{SLIC} = \lvert V_{BAT}\rvert \bullet I_L - P_{RTMG} - R_L(I_L)^2 + 0.12\text{ W}$	Power is dissipated in the SLIC while in Active and Tip Open states.

DC FEED CHARACTERISTICS



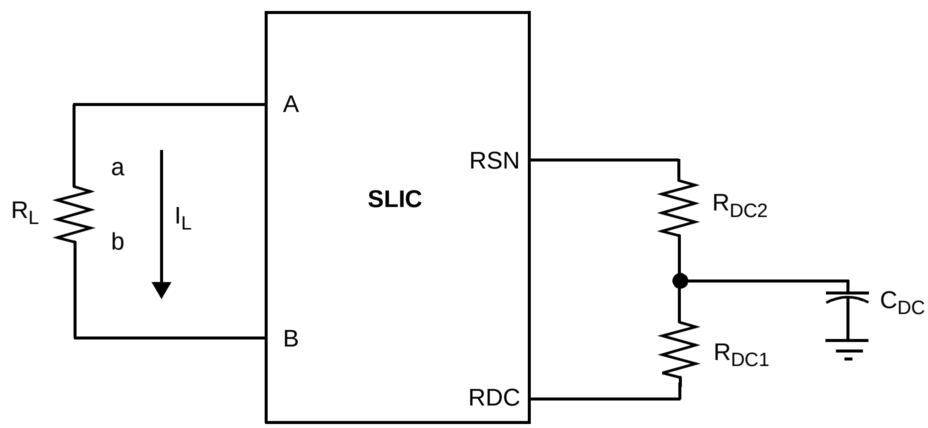
$R_{DC} = R_{DC1} + R_{DC2} = 22.72\ k\Omega$
BAT = –48 V

1. $V_{AB} = I_L R_L' = \frac{500}{R_{DC}} R_L'$, where $R_L' = R_L + 2R_F$

2. $V_{AB} = 0.925 \bullet |V_{BAT}| + 0.9 - I_L \frac{R_{DC}}{120}$

3. $V_{AB} = 0.925 \bullet |V_{BAT}| - 1.83 - I_L \frac{R_{DC}}{120}$

a. Load Line (typical)

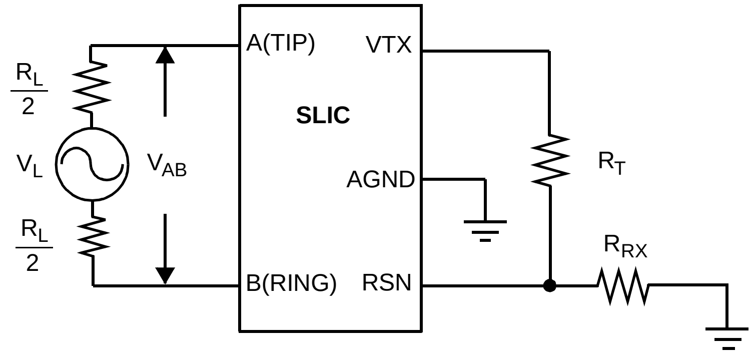


Feed current programmed by R_{DC1} and R_{DC2}

b. Feed Programming

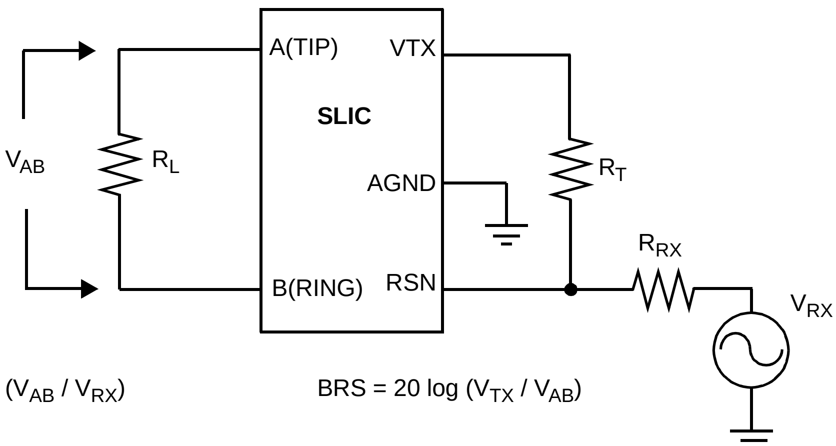
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

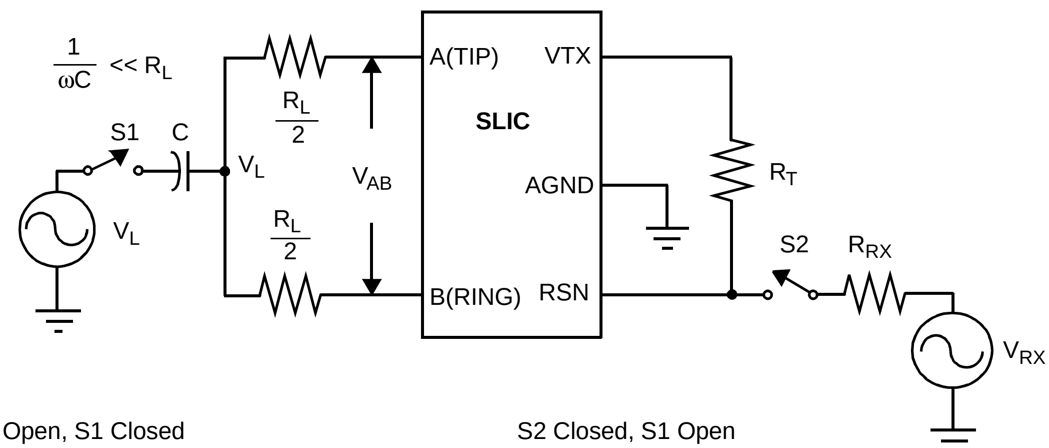
A. Two- to Four-Wire Insertion Loss



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{AB})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed

L-T Long. Bal. = $-20 \log (V_{AB} / V_L)$

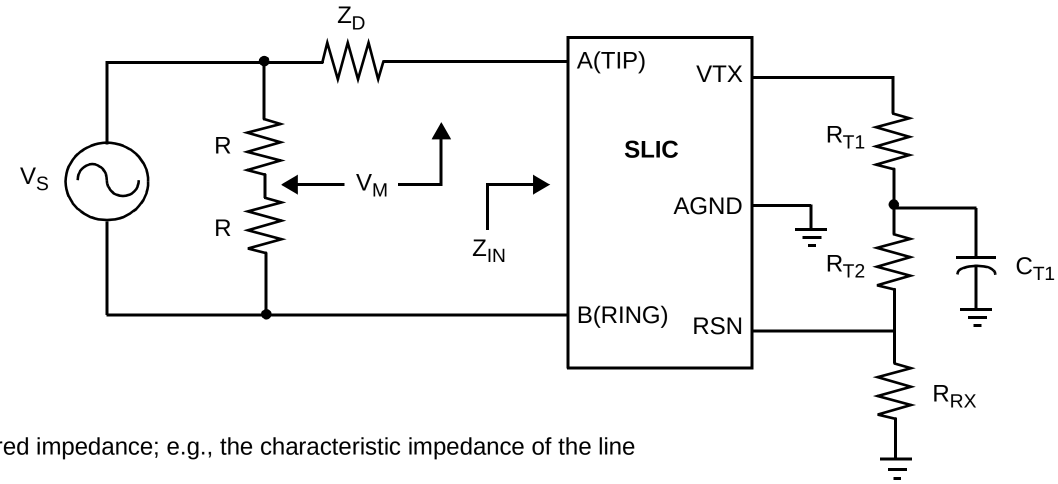
L-4 Long. Bal. = $-20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open

4-L Long. Sig. Gen. = $-20 \log (V_L / V_{RX})$

C. Longitudinal Balance

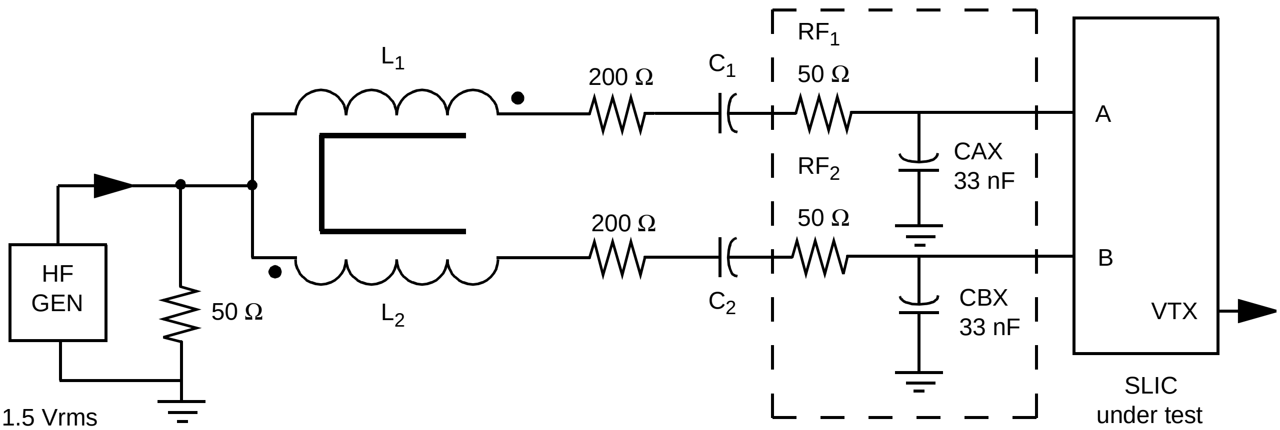
TEST CIRCUITS (continued)



Z_D: The desired impedance; e.g., the characteristic impedance of the line

Return loss = –20 log (2 V_M / V_S)

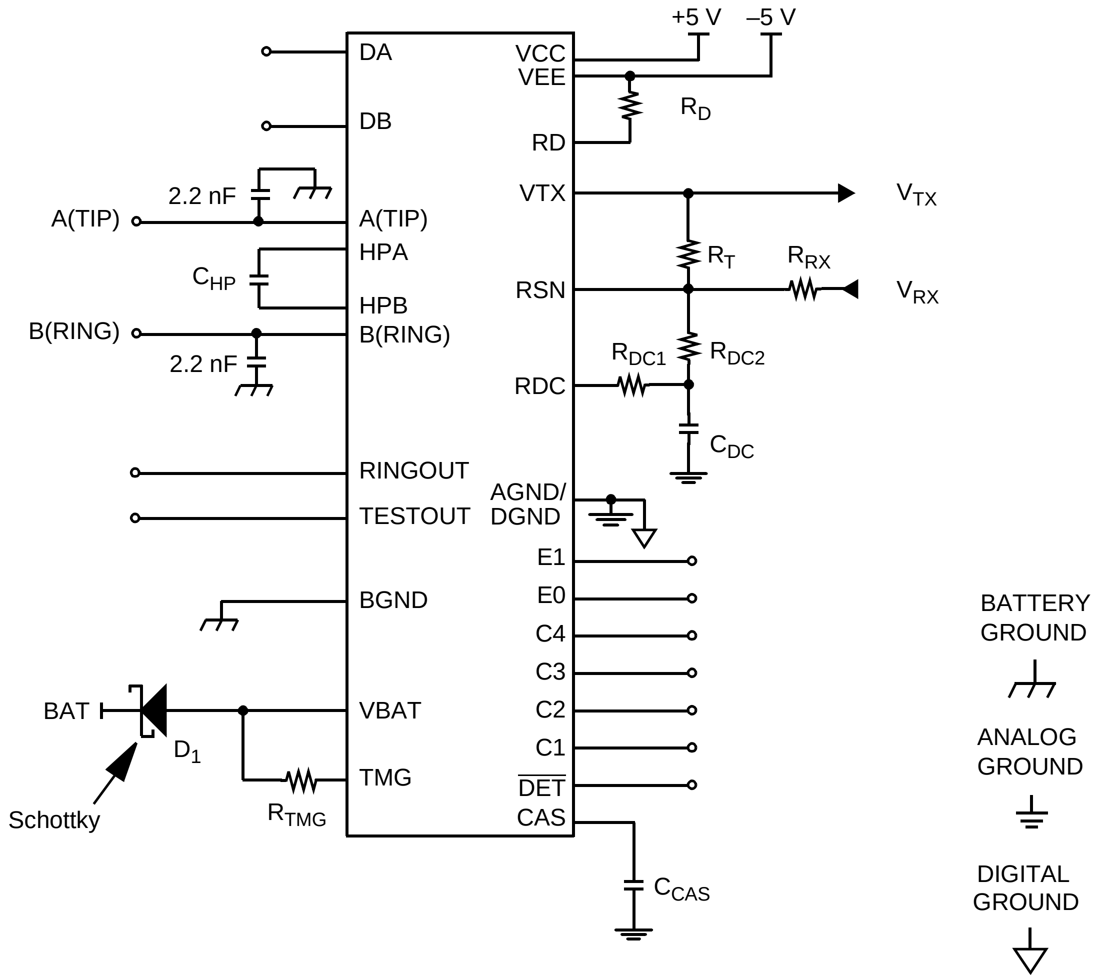
D. Two-Wire Return Loss Test Circuit



1.5 Vrms
80% Amplitude
Modulated
100 kHz to 30 MHz

E. RFI Test Circuit

TEST CIRCUITS (continued)



F. Am79484 Test Circuit

REVISION SUMMARY

Revision A to B

- Within the Electrical Specifications, under the Supply Currents, changed the values for the ICC, On hook VCC Supply Current.
- Minor changes were made to the data sheet style and format to conform to AMD standards.

Trademarks